Low Voltage Swing Logic Circuits for a 7GHz x86 Integer Core

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- Overview of 2x Frequency Integer Core
- Overview of Low Voltage Swing circuits
- Circuit Examples from Integer Core
- Si Results

2x Frequency = Fast CLocK = FCLK

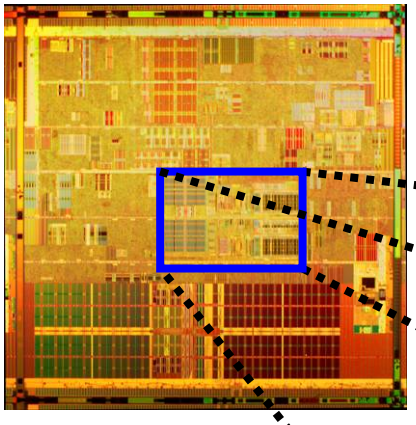
- Twice the core clock frequency of microprocessor
  - On a 3.5 GHz chip the FCLK runs at 7 GHz
  - Fundamental to Intel® Netburst™ Technology
- Logical Depth Available to FCLK circuits
  - FCLK phase has about 6 logic stages best case
  - Subtract clock variation and latch valid/set up times
  - Maybe 2 stages left for logic!
- Very localized use -> exclusive to Integer Core

High Speed Integer Core

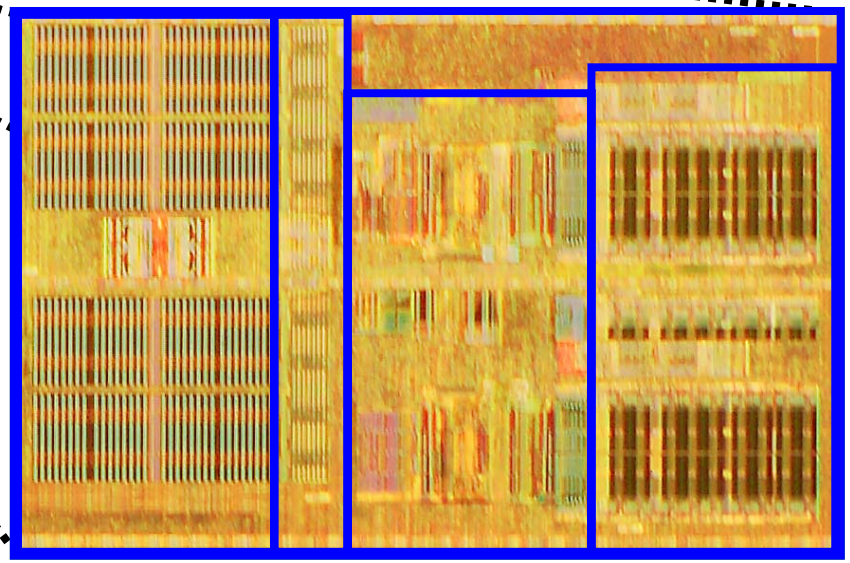
- Fast Integer Data Path (Low Latency Ops)
  - ALUs
  - Bypass Logic
  - Arithmetic Flags
- Integer Register File
- Level 0 Data Cache
- Address Generation Unit (AGU)

Drawn device count exceeds that of a Pentium Pro Microprocessor

We Are Here

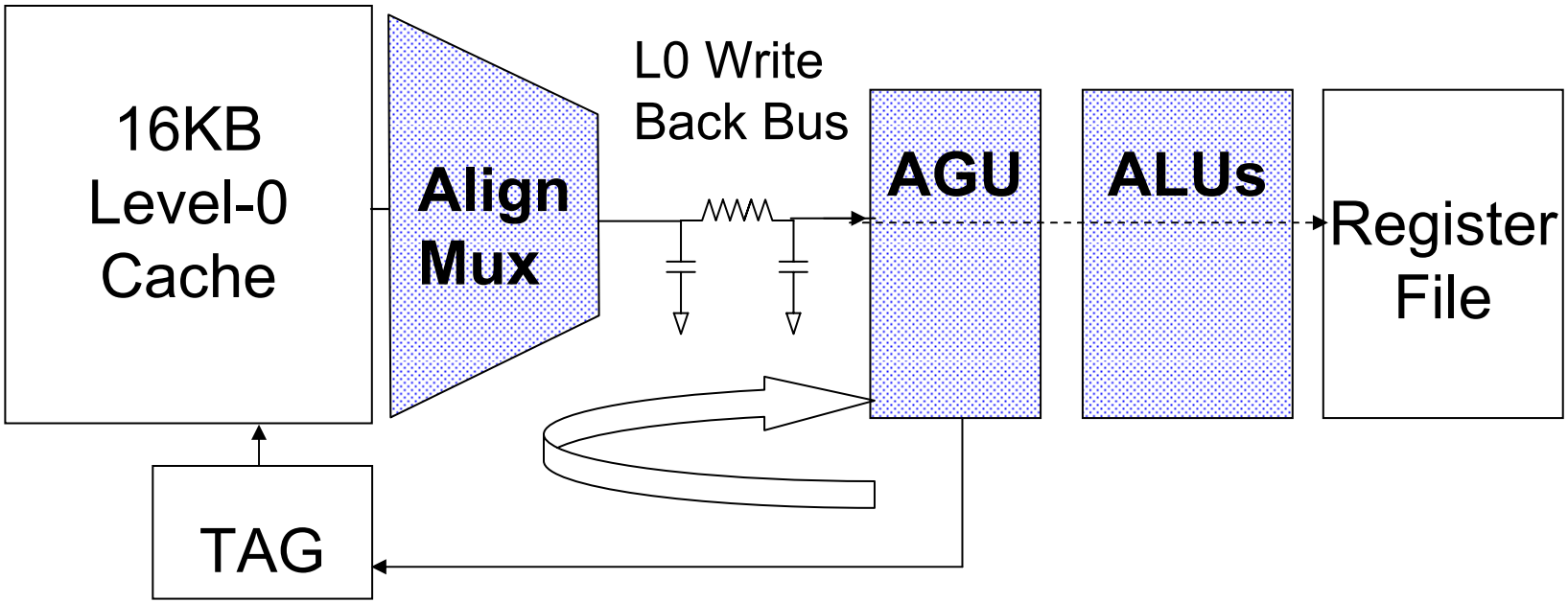


Intel® Pentium® 4 Processor on 90 nm Process



Data Cache | Align Mux | ALUs & AGU | Registers

Integer Core “Loop”



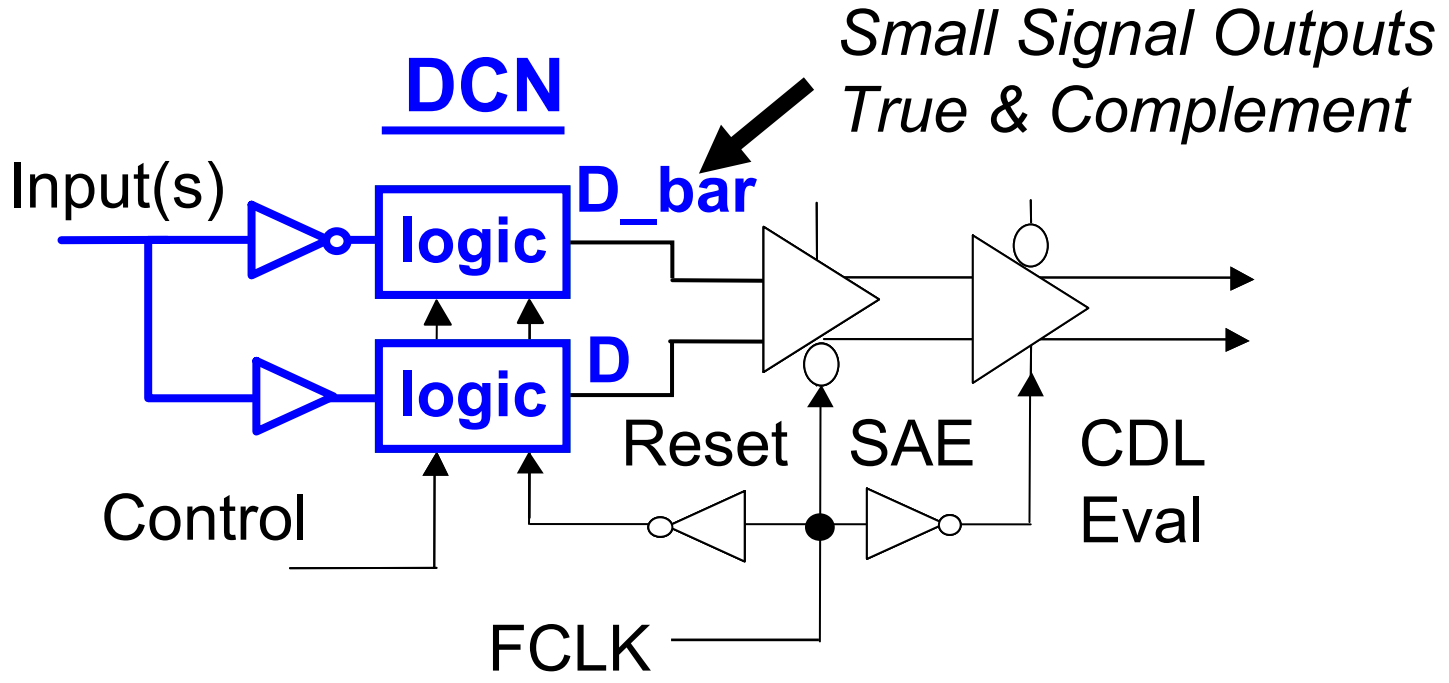
- Critical load pipeline kept short as possible
- Some 16 or 32 bit results needed in a FCLK phase
- Shaded boxes use Low Voltage Swing technology

Low Voltage Swing = LVS

- "A bunch of pass-gates followed by sense-amp"
  - Deep N-passgate logic chains
  - Resulting voltage output is tiny (small signal)
  - Produce true & complement outputs
  - Sense the voltage differential
- Logic functions vary
  - Can be random logic
  - No more than 6 transistors in series
  - No bound for # of parallel connections (function width)

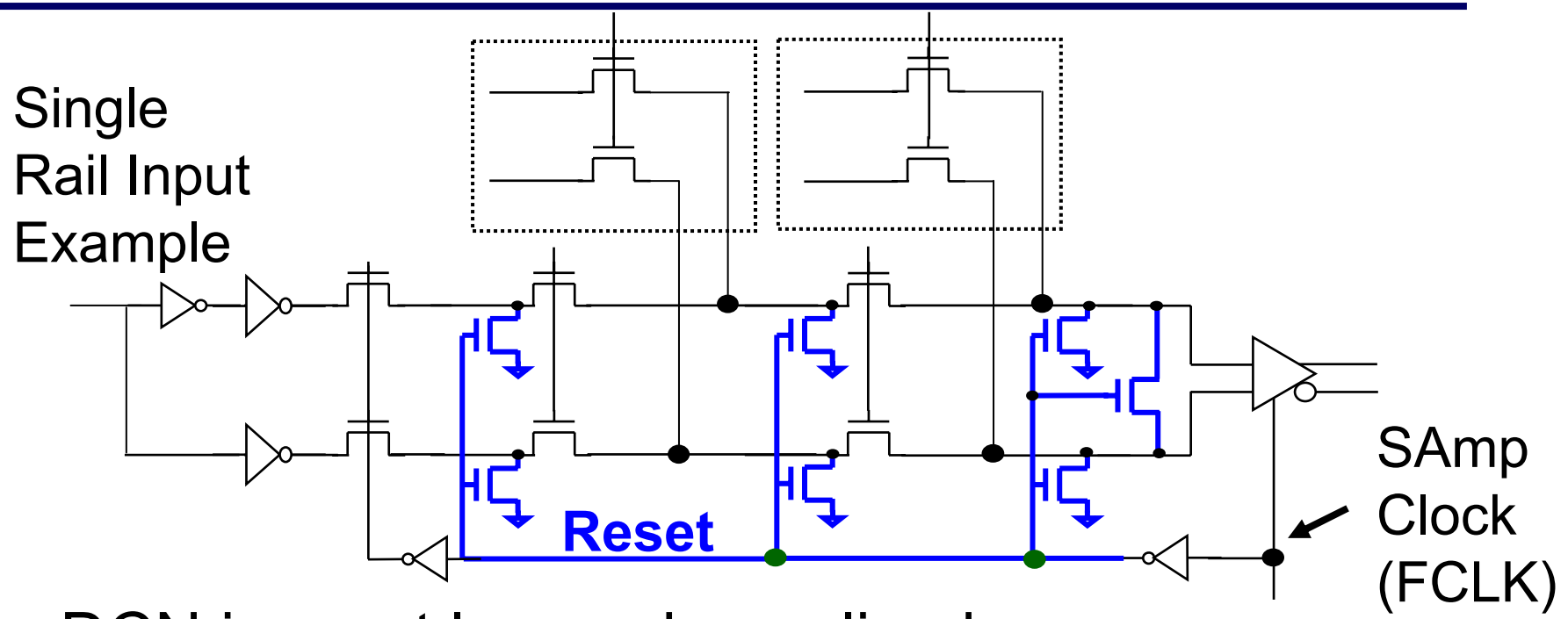
Resulting circuit resembles one big gate with up to 5,000 transistors

LVS Topology: DCN



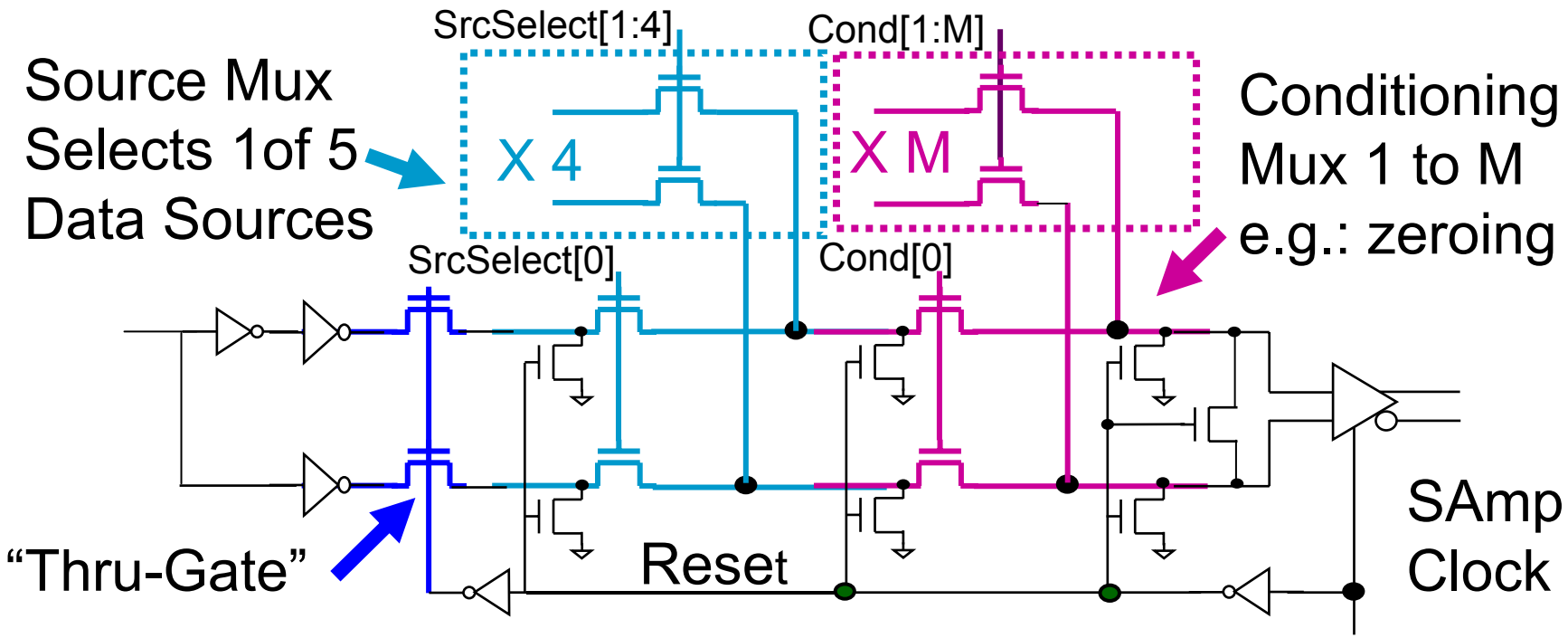
- Inverters drive complementary data into parallel N-channel pass gate logic chains
- Referred to as **D**iffusion **C**onnected **N**etwork (**DCN**)

DCN Example: ALU Source Mux



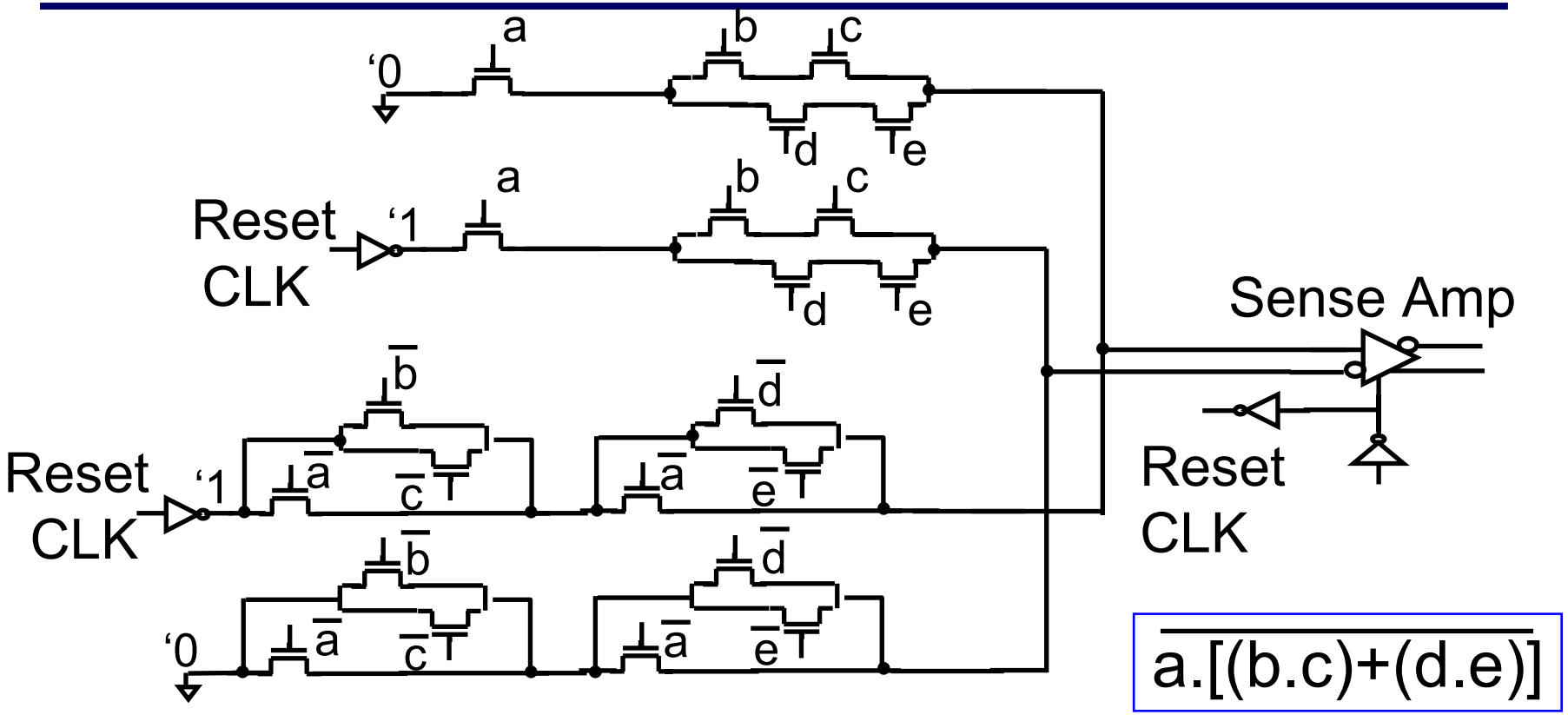
- DCN is reset low and equalized.
- During signal development, one side evaluates high
- Advantages of reset low N-Channel system
  - N vs. P linear region characteristics
  - Minimize capacitance

DCN Control: ALU Source Mux



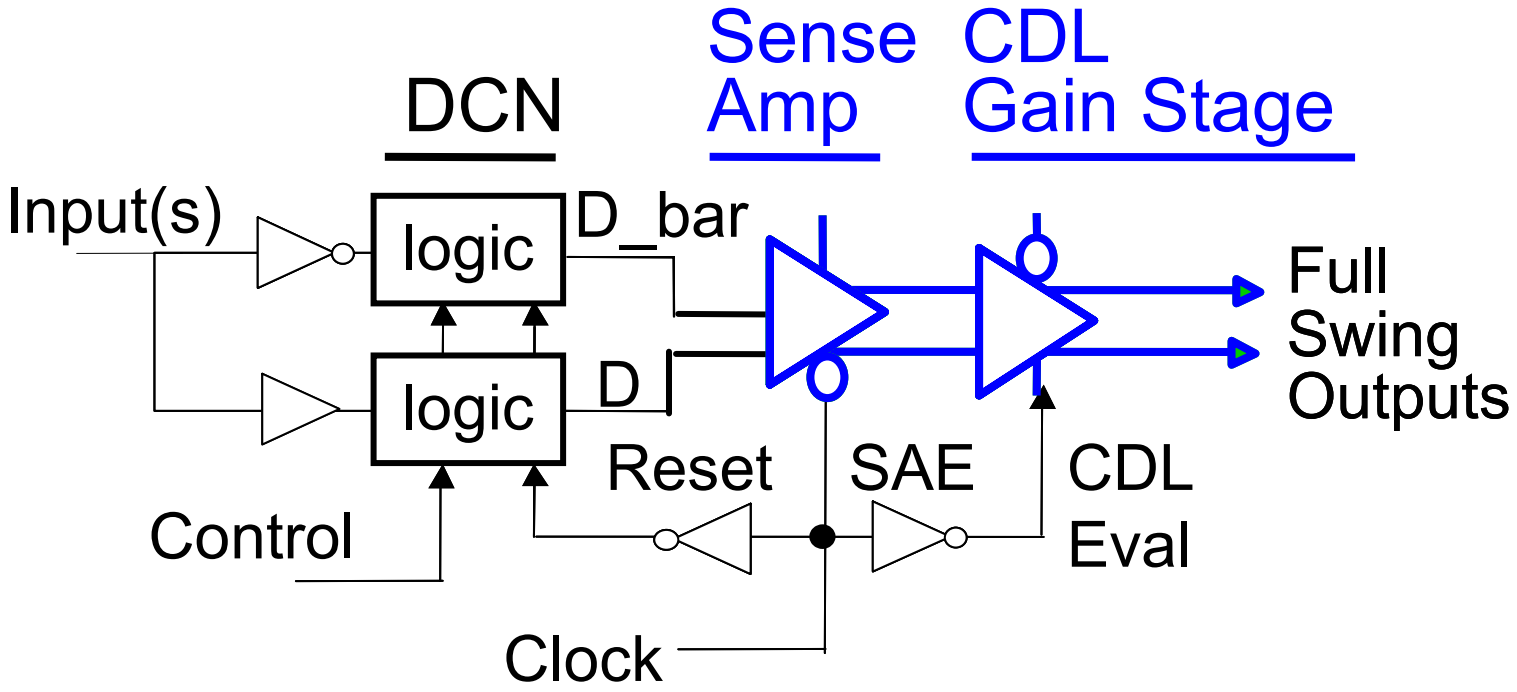
- "Thru-Gate" creates clean static to LVS interface
  - Always reset or qualified by reset
  - Eliminates reset/signal contention
- Other gates (selects) driven by static or domino

DCN: Random Logic Example



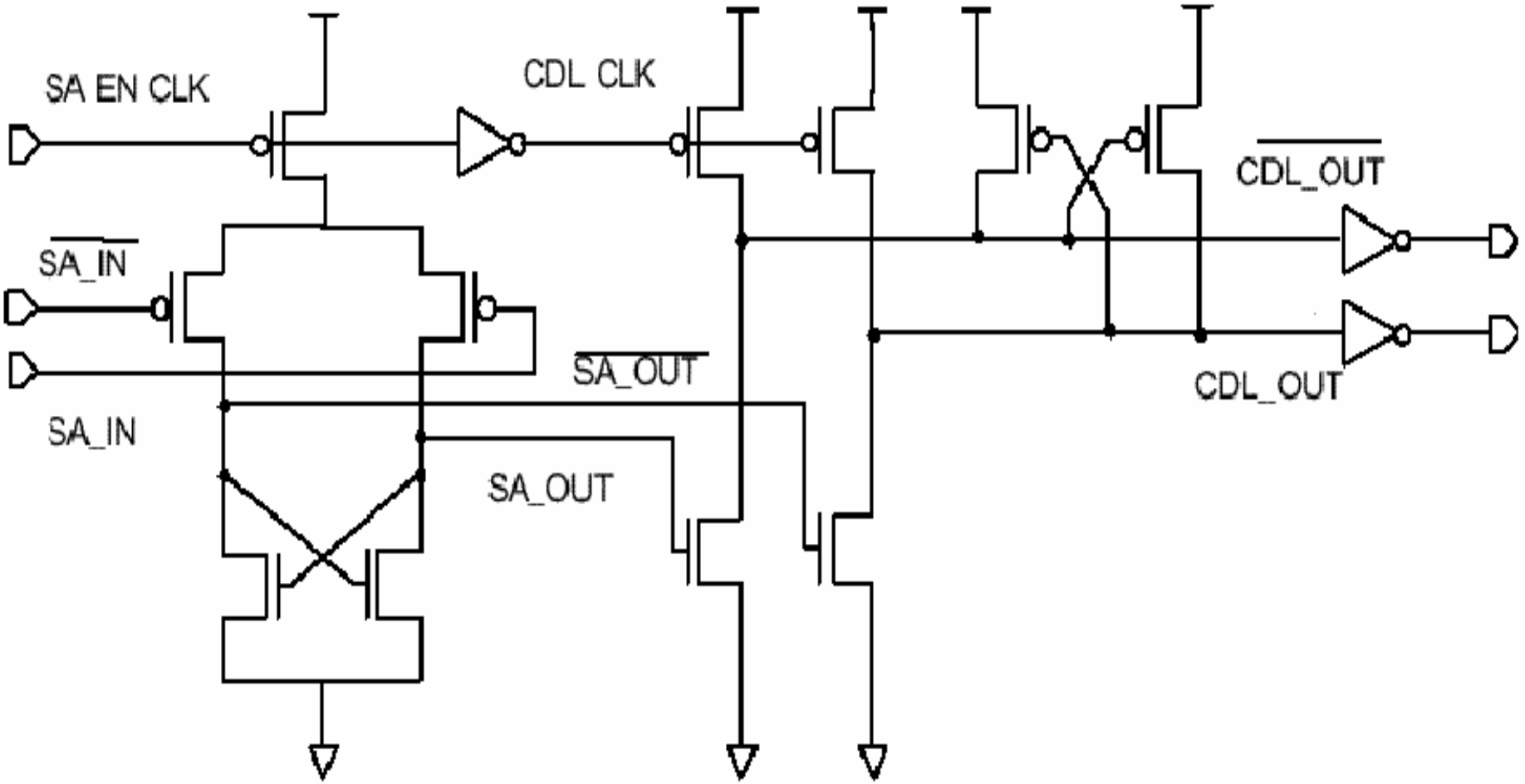
- A complex function illustration (reset not shown)
- Example shows a 3 deep DCN
- Actual circuits have up to 6 devices in series

LVS Topology: Gain

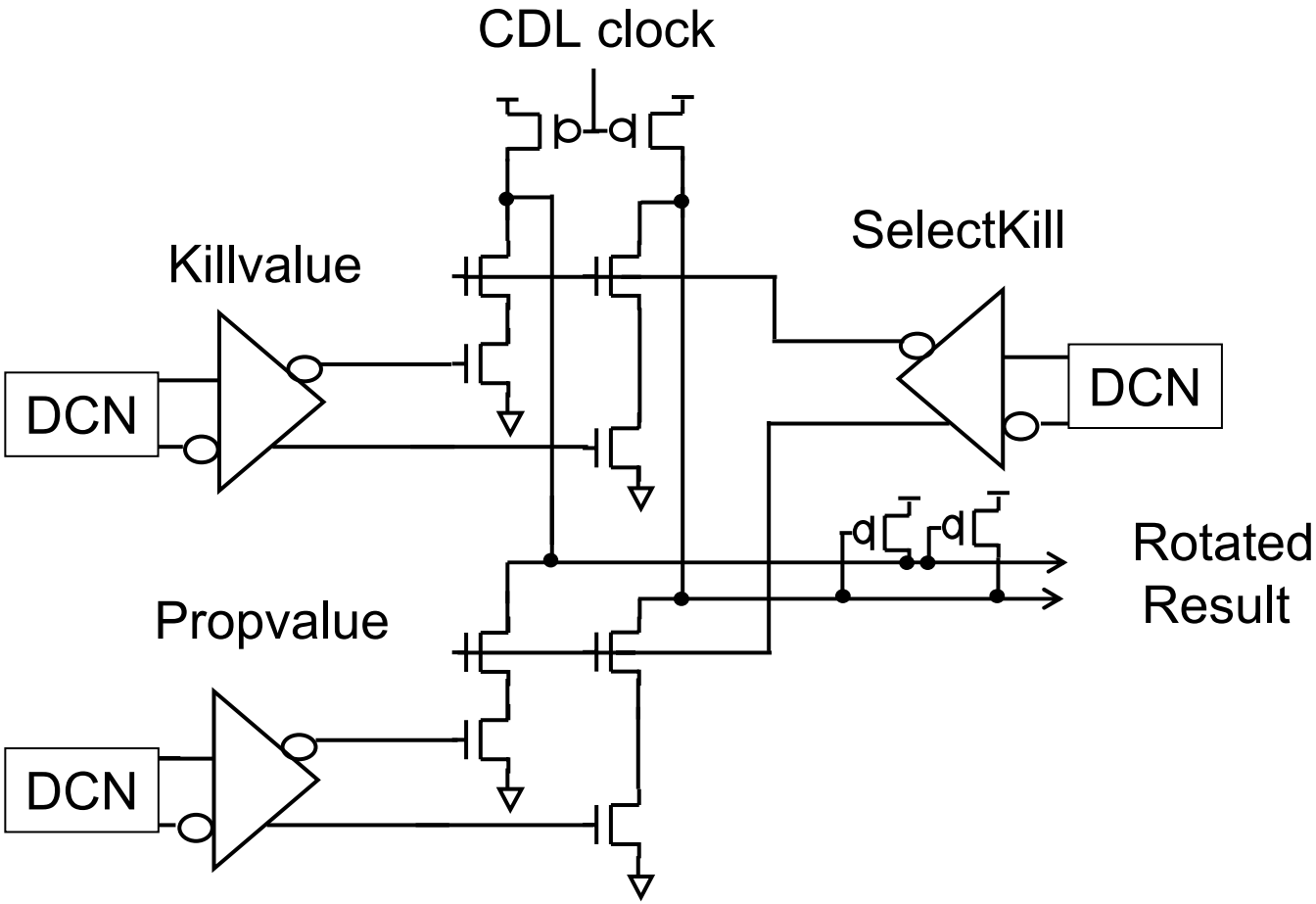


- DCN outputs into a high-speed low-gain ratio'd P sense amp
- Level restore is **C**ross-coupled **D**omino **L**ogic (CDL) gate
- Together these stages amplify 10% VCC differential (average) to full rail

Gain: Sense Amp and CDL



Gain: Complex CDL



- ALU1 Rotator 2-to-1 Mux with Small Signal Selects

LVS: Logical Work Advantage

- Implements up to 7 effective logic stages
  - Up to 6 in DCN and 1 in the CDL
  - Some very wide
  - Wire resistance has very low cost
- Uses less than 4 stage delays of "time"
  - Signal development allocated 2 gate delays
  - Gain stages cost about 2 gate delays

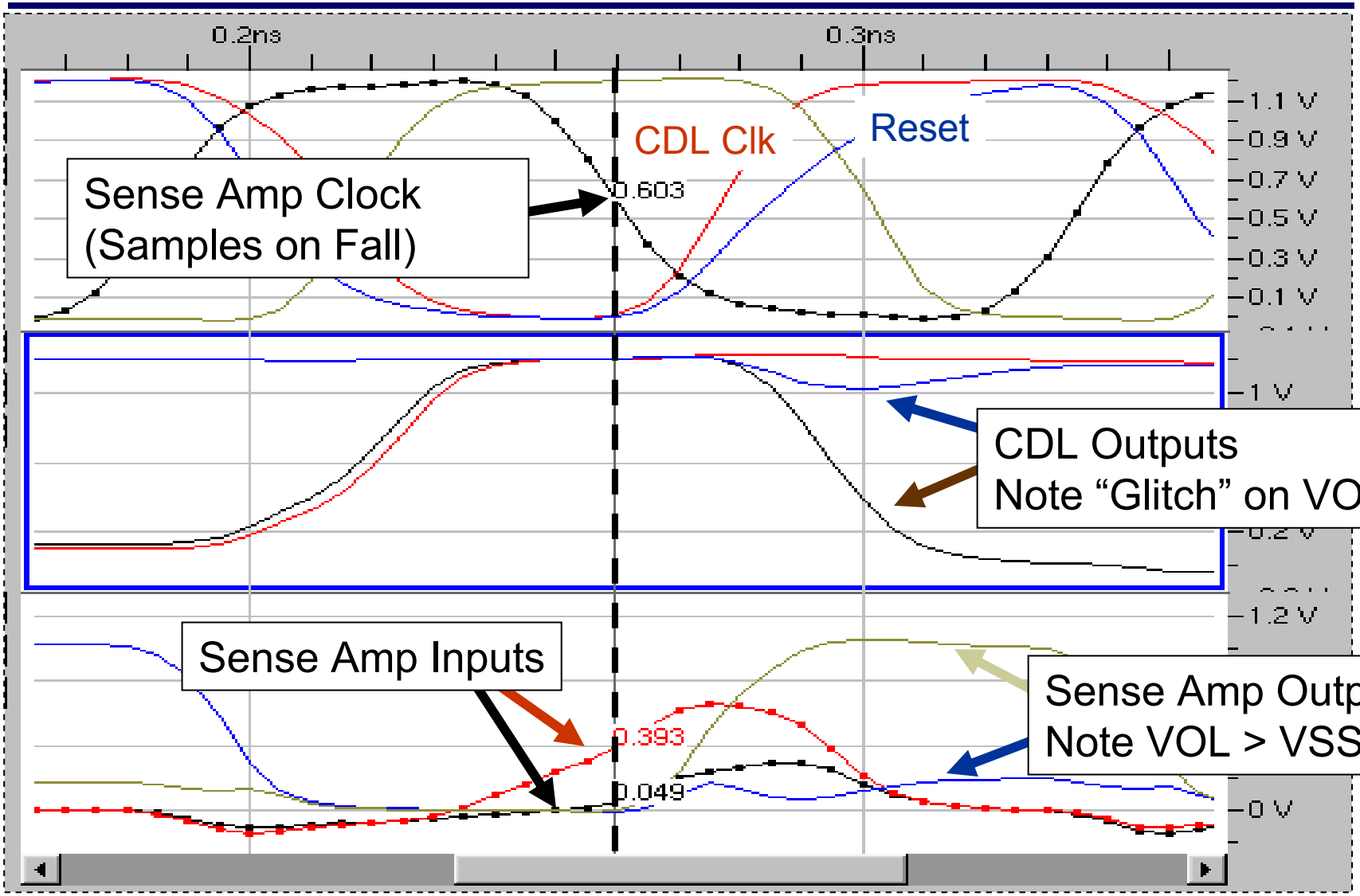
In time of ~4 stage delays ….

…6 to 7 stages of logic is completed

LVS Analysis: Fail Criteria – CDL Glitch

- Sense amp V_{OL} is above V_{SS}
  - Level strongly related to input differential
  - Causes the non-switching CDL output to discharge
  - CDL's cross-coupled P-keepers fight back
  - Below a minimum input differential, the glitch induces a CDL domino false-discharge failure
- Glitch magnitude is a criteria used by in-house tools to calculate the circuit setup time.

LVS Analysis: Simulation Waveforms



LVS Analysis: Fail Criteria – Min Diff

- 2nd criteria is a minimum input differential
  - Differential Noise
  - Sense amp DC offset
  - Process variation
  - Determined for each circuit
  - Typically 8-10% supply
- Either of two criteria can dominate – depends on the circuit being analyzed

LVS Analysis: Verification

- In house tool exhaustively traces all circuit paths
  - Path pruning is guided by logic equations attached to schematic nodes
  - RTL has equivalent logic equations
    - Formally verified against each other
    - RTL equations are proven in our logic validation suite
- Post pruning ALU1 Rotator has ~42,000 traces!
- Trace count increases 10x further when tool includes all differential noise scenarios

LVS Analysis: Noise Worries

- Noise analysis is not fool proof
  - 10x trace explosion is too much for every tool run
  - Simplifying assumptions need to be made
  - Best to design “correct by construction”
- Matching analog layout rules required
  - 3 dimensions thru layer above last small signal
  - In-house analog layout rule checker was built to enforce adherence to matching rules
  - Essentially random logic is proven, by construction, to have minimal differential noise

LVS Structures

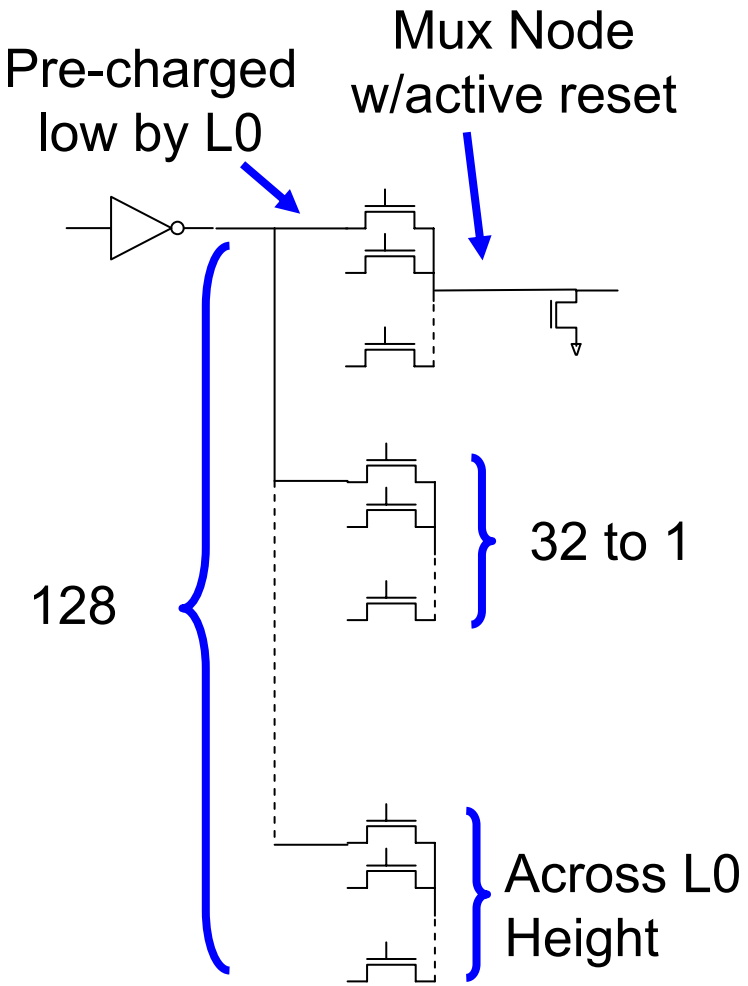
- L0 Data Alignment mux
  - Novel core clock structure delivering FCLK thru put
  - 32:1 L0 data alignment in less than 1 FCLK phase
- Arithmetic Logic Unit 0 (ALU0)
  - 32 bit adder & 32 bit integer Boolean logic functions
  - Adder implemented as carry select topology
- Arithmetic Logic Unit 1 (ALU1)
  - 32 bit adder & fast 32 bit integer shift/rotate
  - Fast shift/rotate is new to architecture
  - Shares the adder design of ALU0

LVS Core Structures (cont'd)

- Address Generation Unit (AGU)
  - 4 phases back-2-back LVS doing address calculations
  - Several ALU based adders/carry chains
- These 4 LVS structures make up over 20% of Integer Core

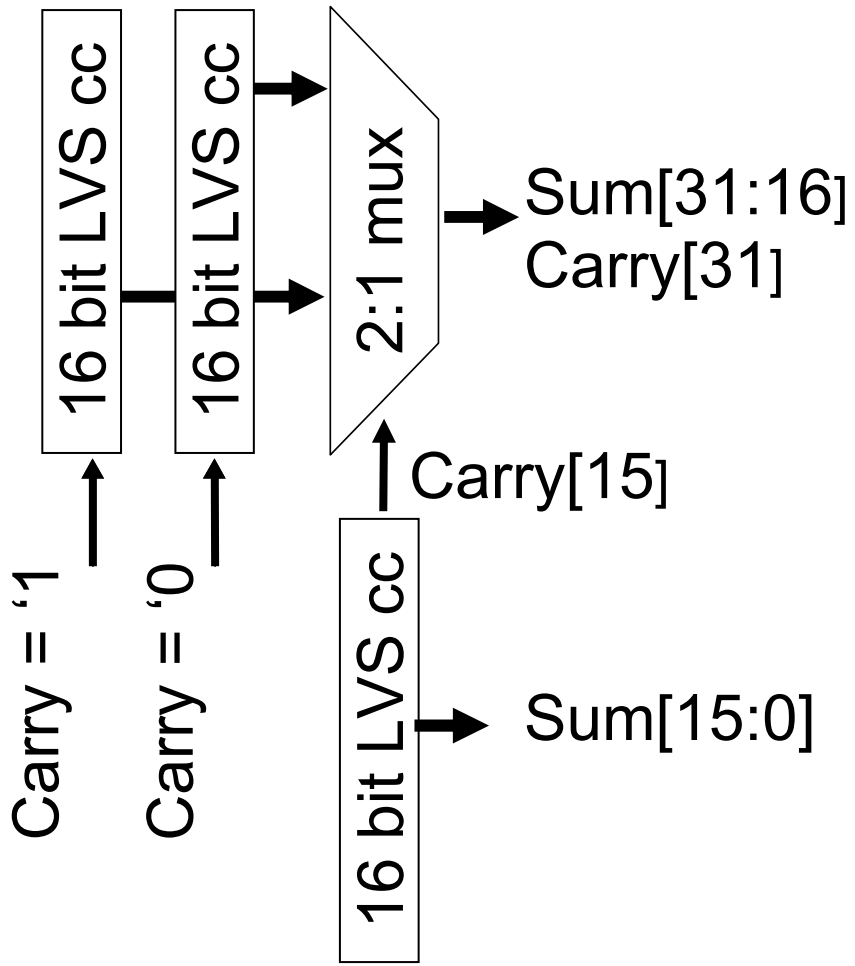
LVS Align Mux Topology

- LVS enables non-traditional implementation
- 128 individual 32 to 1 dual rail muxes
- Single logic stage
- Mux node distributed over the height of the L0
- Large R & C of mux node results in small signal
- True & complement mux nodes differentially sensed

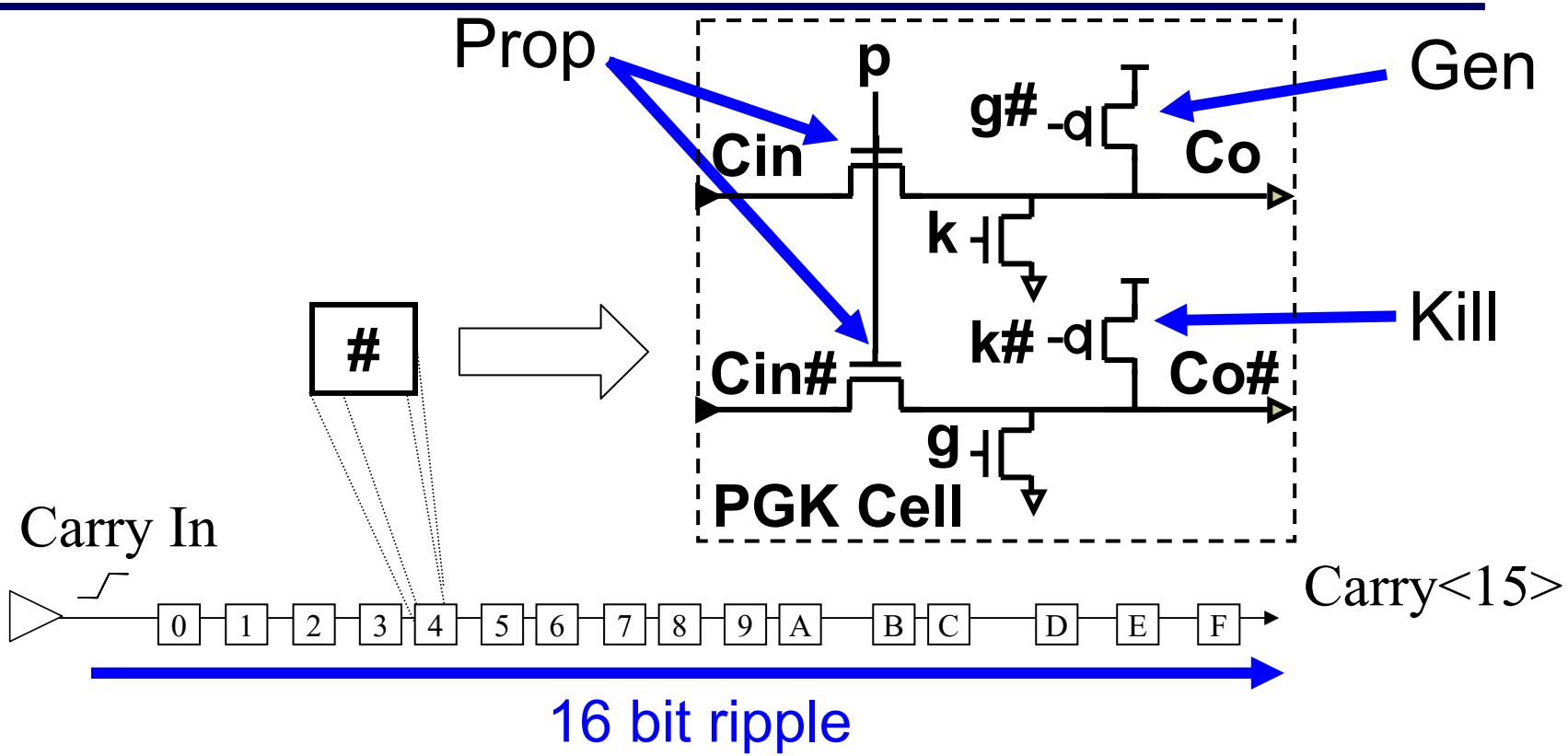


LVS Adder Topology

- LVS allows long simplistic ripple carry chains
- Only one FCLK phase to evaluate
- Carry propagation for 32-bits is too slow for FCLK
- Use 3 16-bit LVS adders in carry-select configuration
- All ALU & AGU adders built upon same 16-bit LVS adder configuration

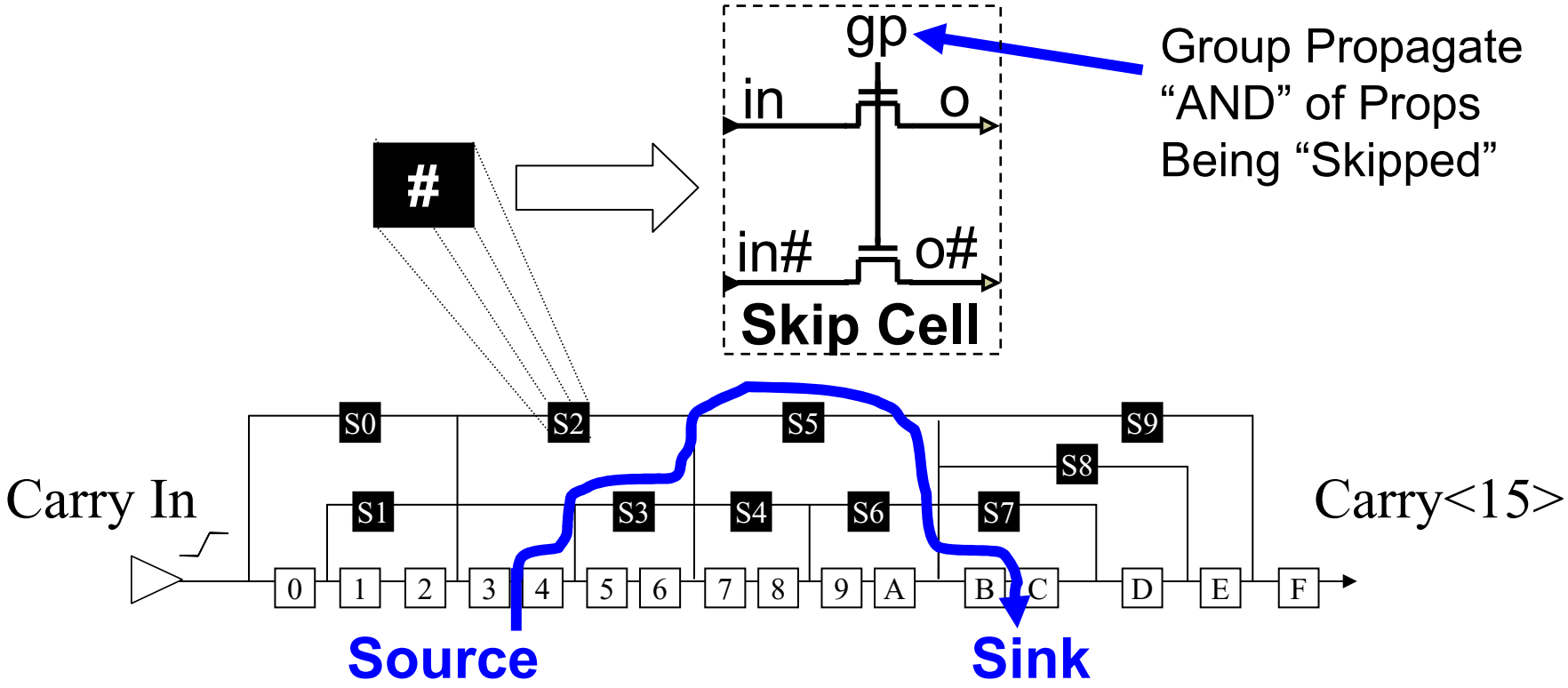


LVS Carry Chain: 16 bit add



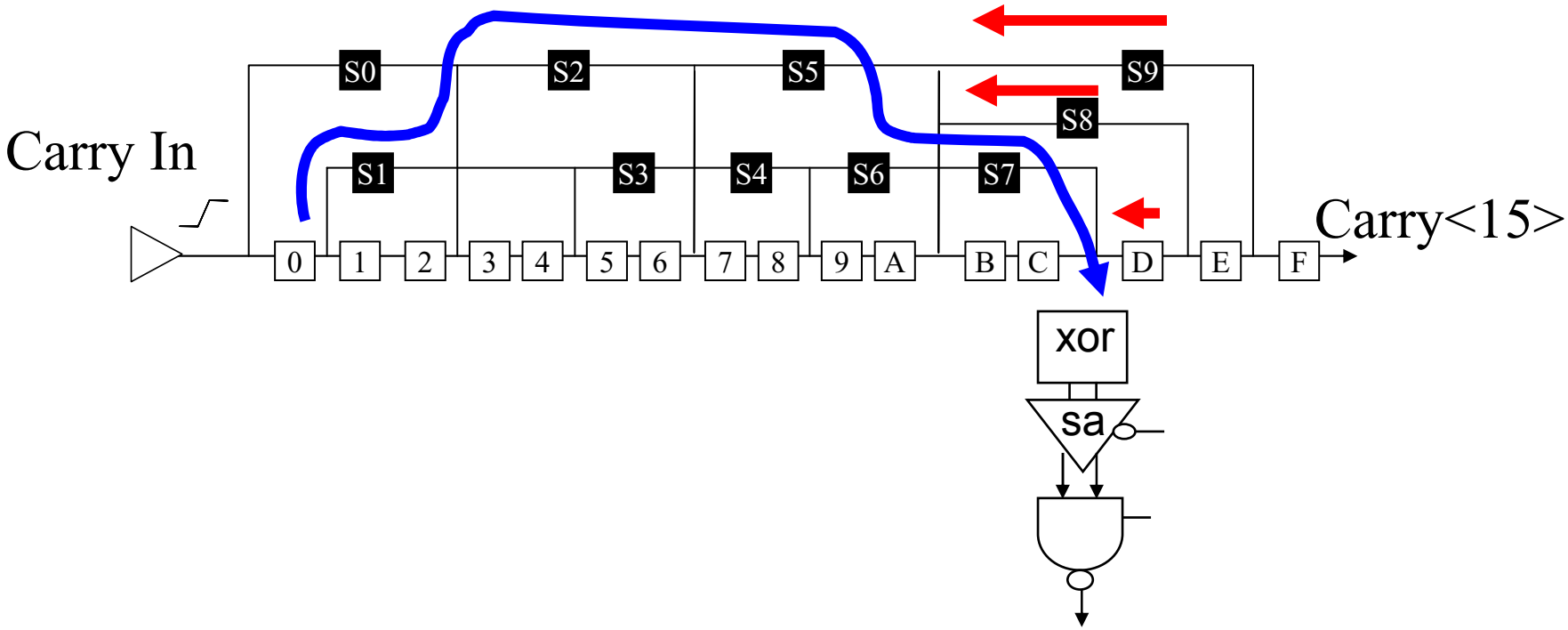
- Cascaded PGK cells - any point can generate or kill
- gen/kill devices double as reset devices
- Without skips this DCN has up to 16 devices in series

LVS Carry Chain: Skip



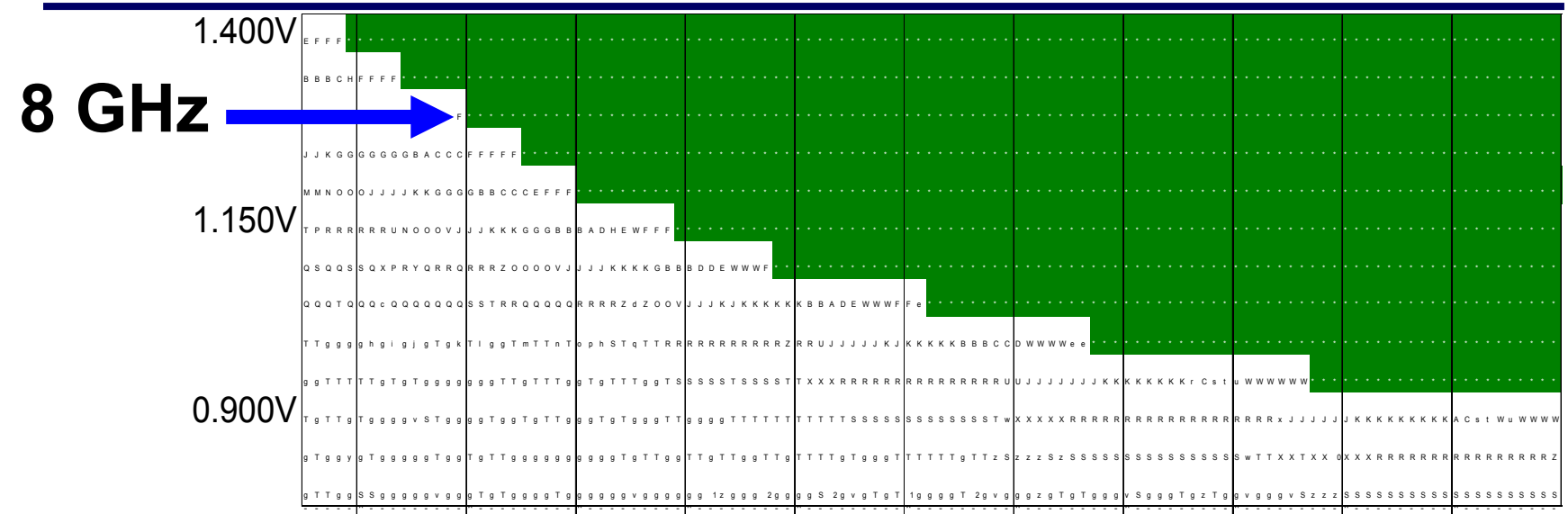
- Arranges skips so source-2-sink path is <= 6 series devices
- Group Propagates are start of a typical critical path
- N pass gate XORs at carry[n] node produce sum [n+1]
- Further optimizations can reduce to <= 5 series devices

LVS Carry Chain: Attackers



- Driver is “far” away at bit 0 -> poor response
- Multiple attackers at 10 & 12 “near” to Sense Amp
- Back-contention can cause freq independent failures
- The In-house noise/timing tool runs these scenarios

Si Data: Integer Core V vs. Freq



Bus Per (ns)	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5
Part Freq (MHz)	4211	4000	3810	3636	3478	3332	3200	3077	2963	2857	2759
2x Core Freq (MHz)	8422	8000	7638	7272	6956	6664	6400	6154	5926	5714	5518

- Fabricated on 90nm technology
- Volt-Freq Shmoo of isolated FCLK (2x freq) Integer Core showing 8GHz, 70C, 1.3V (450 directed patterns)
- Design has headroom to scale with process improvements

Conclusion

- Low Voltage Swing technology delivers very high frequency circuits
  - Enables the 2x frequency integer core of Intel® NetBurst® microarchitecture
  - Targeted for Intel® Pentium® 4 processors in Intel® 90nm process
  - Post Silicon results of the integer core hit frequency expectations with headroom to scale further with the process